Status of Claims after this Response:

1. (Currently Amended) An integrated circuit wafer comprising:

a substrate comprising a wafer material, said substrate having first and second surfaces, said first surface having a circuit layer comprising integrated circuit elements constructed thereon, and extending a maximum distance from said first surface into said substrate such that all of said integrated circuit elements are located between said first surface and said maximum distance;

a plurality of vias extending a first distance from said first surface of said substrate into said substrate, said first distance being less than the distance between said first and second surfaces of said substrate said first distance being greater than said maximum distance, said vias having a bottom surface comprising a stop layer covering said bottom surface, said stop layer comprising a stop material that is more resistant to ~~chemical/mechanical~~ removal by polishing ~~(CMP)~~ than said wafer material, said stop layer not being part of any of said integrated circuit elements.

2(Original). The integrated circuit wafer of Claim 1 wherein said stop material comprises a material chosen from the group consisting of Ta, TaN, W, WN, $Ta_xSi_yN_z$, W_2, and Si_yN_z, and wherein said wafer material comprises silicon.

3(Original). The integrated circuit wafer of Claim 1 wherein said vias are lined with a layer of an electrically insulating material.

4(Original). The integrated circuit wafer of Claim 3 wherein said electrically insulating material comprises SiO_2.

5(Original). The integrated circuit wafer of Claim 3 wherein said vias are filled with an electrically conducting material.

6(Original). The integrated circuit wafer of Claim 5 wherein said electrically conducting material comprises an element chosen from the group consisting of copper, tungsten, platinum, and titanium.

7. (Currently Amended) An integrated circuit wafer comprising:

a substrate comprising a wafer material, said substrate having first and second surfaces, said first surface having a circuit layer comprising integrated circuit elements constructed thereon, and extending a maximum distance from said first surface into said substrate such that all of said integrated circuit elements are located between said first surface and said maximum distance;

a plurality of vias extending a first distance from said first surface of said substrate into said substrate, said first distance being less than the distance between said first and second surfaces of said substrate said first distance being greater than said maximum distance, said vias having a bottom surface comprising a stop layer covering said bottom surface, said stop layer comprising a stop material that is more resistant to ~~chemical/mechanical~~ removal by polishing ~~(CMP)~~ than said wafer material, said stop layer not being part of any of said integrated circuit elements;

a dielectric layer having top and bottom surfaces, said dielectric layer covering said circuit layer such that said bottom surface is in contact with said integrated circuit layer; and

a plurality of electrical conductors buried in said dielectric layer and making electrical connections to said integrated circuit elements.

8(Original). The integrated circuit wafer of Claim 7 wherein at least one of said vias extends through said dielectric layer and wherein said one of said vias is filled with an electrically conducting material, said via terminating in an electrically conducting pad on said top

surface of said dielectric layer.

9(Original). The integrated circuit wafer of Claim 8 wherein said electrically conducting pad extends above said top surface of said dielectric layer.

10(Original). The integrated circuit wafer of Claim 8 wherein one of said electrical conductors is connected electrically to said one of said vias.

Claims 11-16 have been withdrawn in response to a restriction requirement.

17. (New) The integrated circuit wafer of Claim 1 wherein said maximum distance is between 4 and 9 microns.